Part III Project Report

Electrically contacting nanocrystals using a selectively etched nanogap

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Abstract

The study of nanoparticles and their electrical properties has emerged in recent years as a major forefront of condensed matter physics whose implications range from fundamental physics to electronic device applications. In order to be integrated in electrical circuits, effective and reliable ways of contacting nanoparticles have to be developed. This project is focused on investigating the properties of a device which uses the process of self-assembly, combined with lithography techniques to create such a contact. I measured and classified the observed types of I-V characteristics and performed data analysis on the acquired data in an attempt to find the optimal nanocrystal solution and contact design.

Contents

1 Introduction

The electrical properties of macroscopic semiconductor crystals are well described by the band structure of the material. It consists of the continuous sets of energy states separated by the band-gap energy E_g which characterises the semiconductor. It is shown on the example of PbS, the material our nanoparticles are made of, in Fig.(1).

However, for small crystals with size comparable to the length scales of electronic energy transfer, the standard band structure theory no longer applies. One of these length scales is the de Broglie wavelength of electrons giving us the value $\lambda \approx 20$nm at room temperature. A nanocrystal of that size can be considered a quantum dot, tightly confining a small number electrons or holes and leading to discretization of energy states. As a consequence, the crystal exhibits a variety of new phenomena. The confluence of several technologies now allows for the routine fabrication and study of these semiconductor structures [12].

The potential of using the unique properties of nanocrystals in new technological applications has been discussed in many fields, such as nanoelectronics, photovoltaics, and optoelectronics [3]. One of such applications is a possible improvement over the existing transistors. Molecules or nanocrystals with sizes smaller than 10nm and suitable properties can already be made, but in order to be integrated in circuits an electrical contact at both sides of the molecule must be made. My project was based on making measurements and characterising properties of a device which uses a process of self-assembly combined with lithography techniques to establish such a contact.

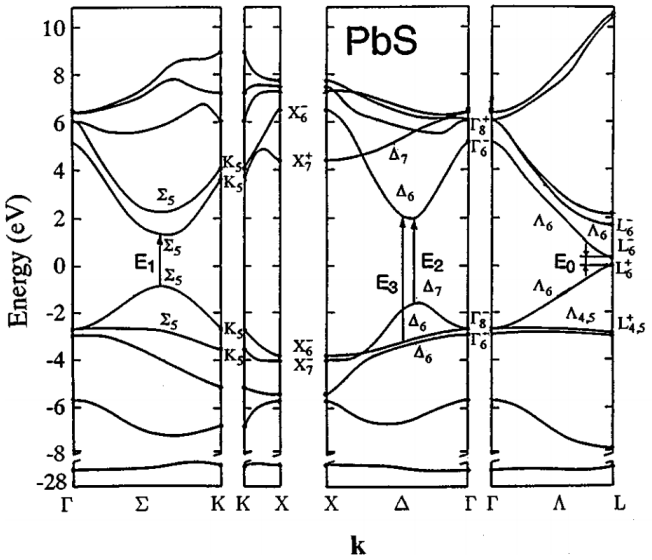

Figure 1: Band structure of PbS as calculated by S.E. Kohn *et al.* [10] and taken from Ref. [9]

2 Background Theory

The nanocrystals we are using have a diameter of about 5nm and are thus sufficiently small to be modelled as quantum dots up to a good precision. When put between two electrodes they can be modelled as potential wells, separated by tunnel barriers from source and drain. Energy conservation and Fermi statistics dictate when a given tunnelling process is possible and hence when current can flow [4].

The charge trapped in the potential well is quantised as $q = -eN$ and is not necessarily completely screened by the background positive charge. This gives rise to a charge difference Δq between the negative electron charge and positive background. Trying to remove or add an electron costs Coulomb charging energy $(e^2 + 2e\Delta q)/2C$ where C is the capacitance of the quantum dot to the rest of the world. Tunnelling is hence suppressed and we get an effect known as Coulomb blockade. In practice, however, the criterion $k_B T < e^2/C$ has to be met in order for single-electron charging effects to be observable. In submicron dots ($C \sim 10^{-17} F$) and in liquid helium temperatures (4K) as in our experiment, this is easily attainable.

Adding a possible surface gate and the fact that the energy states are discretized, we can write the total energy of a dot containing N electrons as:

$$U(N) = \sum_{i=1}^{N} E_i + \frac{(-eN + C_g V_g)^2}{2C} \tag{1}$$

where E_i is the single-particle energy of the i^{th} state, C_g is the capacitance between the dot and the surface gate, V_g is the gate voltage and C is the total capacitance. Therefore, the energy required to add the N^{th} electron to the dot is given by the electrochemical potential:

$$\mu_d(N) = U(N) - U(N-1) = E_N + \frac{(2N-1)e^2}{2C} - e\frac{C_g}{C}V_g \tag{2}$$

Changing the number of electrons in the nanocrystal changes the electrochemical potential by:

$$\mu_d(N+1) - \mu_d(N) = E_{N+1} - E_N + e^2/C \tag{3}$$

Therefore, when the electrochemical potentials of the current leads are in between the electrochemical potentials of the states N and $N+1$ (Fig.(2)), electrons cannot tunnel into the dot and the current is strongly suppressed. Moreover, from formula 3 we can see that the effect of the gate voltage is to raise or lower the electrochemical potential of the states in the dot. Hence, applying the appropriate voltage will lift or impose the Coulomb blockade leading to the conductance as shown in Fig. (3). This level of control over conductance, combined with their small size is what makes nanoparticles a good candidate for future transistors.

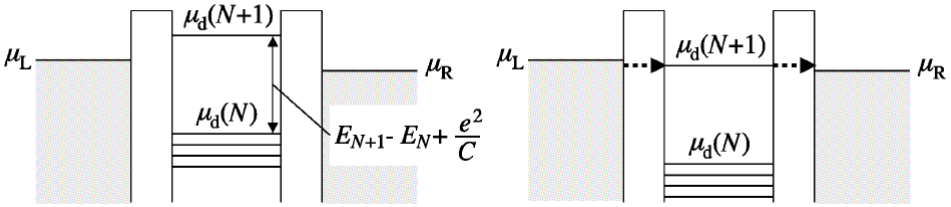

Figure 2: Coulomb blockade in a quantum dot: (a)no energy levels between source and lead electrochemical potentials, tunnelling suppressed (b)electrochemical potential of the $(N+1)^{th}$ state between source and lead electrochemical potentials, tunnelling possible. Picture from PNS course [4]

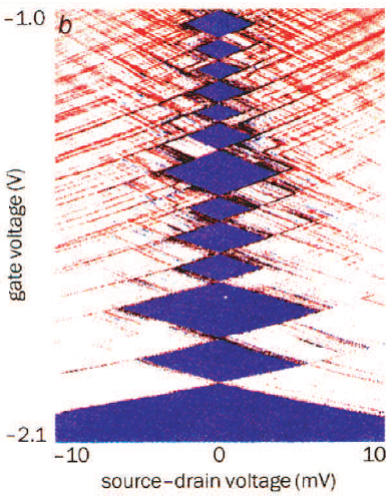

Figure 3: Grey-scale plot of the conductance of quantum dot dependant on gate voltage and source/drain voltage. Lighter regions imply higher conductance. Picture from PNS course [4]

A particularly interesting example of single-electron charging on I-V characteristic of a QD can be seen when one tunnel barrier is significantly more transmitting than the other. This leads to the characteristic referred to as the Coulomb staircase (Fig. (4)). Unlike the Coulomb suppression of current in the neighbourhood of $V_{ds} = 0$, the staircase is not a universal feature of the Coulomb blockade, but a special effect arising when the tunnelling rates between source and drain are very different [12]. The exact current can be calculated for given capacitances and tunnelling rates by solving for a stationary state of a set of balanced tunnelling rate equations [8].

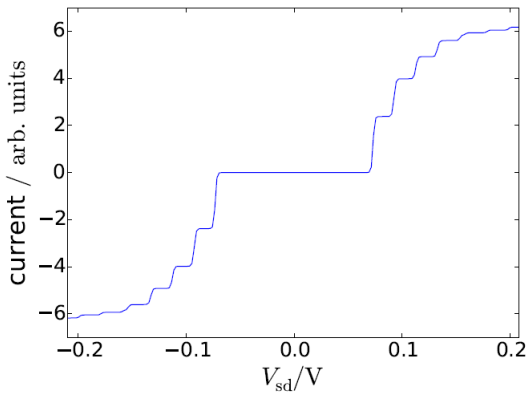

Figure 4: Idealised example of Coulomb staircase I-V diagram

2.1 Graphene

Graphene was discovered in 2004 [15] and its unique properties have become an active area of research ever since. Firstly, it is the first two-dimensional crystal discovered. It is also a semi-metal, a semiconductor with zero band gap energy (Fig. (5)) with remarkably high electron mobility of 200,000cm^2/Vs in suspended graphene [2]. Moreover, it has been measured by C. Lee *et al.* that the Young modulus of graphene is 1.0TPa making it the strongest known material.

Graphene's properties make it a great candidate for the top electrode in vertical device architectures where a layer of molecules or nanocrystals is being contacted. Metal evaporation was found to give poor results due to shorting by evaporation between the particles and sometimes even damaging the particles [6]. On the other hand, graphene provides us with a stable, light and highly conducting electrode which can be deposited without shorting the device.

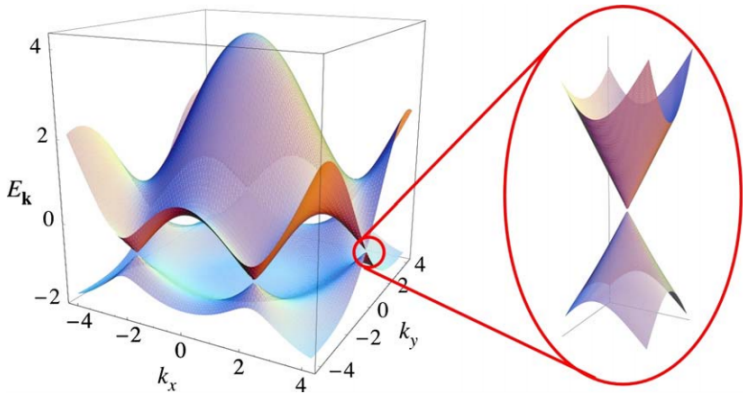

Figure 5: Graphene dispersion relation with zoom in of the energy bands close to Dirac point. Picture from Ref. [14]

A single layer of graphene is deposited by a method known as wet transfer. A layer of graphene is grown on Cu using chemical vapour deposition (CVD) growth process. It is then coated with PMMA optical resist and left in an ethcant which eliminates copper. The residue is put in water and, as PMMA is hydrophobic, graphene will be facing down. A transfer is preformed by fishing the floating graphene with the device.

3 Device Architecture

3.1 Nanogap Device

The initial idea for the project was based on the device designed by Q. Miao which attempted to use a selective-etching technique on GaAs sandwich structure to create 6nm electrodes able to accommodate 4.6nm CdSe nanocrystals. The selective-etching technique is based on the different etch rates of materials. A GaAs-AlAs-GaAs sandwich structure is fabricated using Molecular Beam Epitaxy (MBE) and then etched by buffered hydrofluoric acid. The acid etches out the middle 6nm AlAs isolating layer, while leaving the outer layers intact (Fig. (6)).

Once it has been developed and tested for shorts, the chip is dipped in a solution containing CdSe nanocrystals. It is expected that some of the nanocrystals are going to bridge the gap between the GaAs layers making the device conduct.

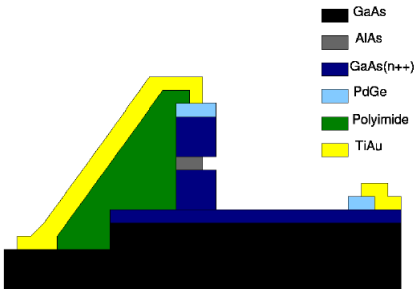

Figure 6: Device cross-section after processing and etching of the AlAs layer. Picture from Ref. [13]

Initial measurements on these devices have been made and it has been shown that the current scales after exposing to CdSe solution are 10-1000 times bigger. However, single-electron phenomena as described in the Section (2) were not observed. This was not unexpected as nanocrystals were allowed to attach on any part of the pillar, most likely resulting in many conducting particles. As crystals are not all exactly the same, the resulting effect is expected to make the I-V diagram smoother and the Coulomb staircase no longer visible.

I was supposed to make measurements of the new generation of devices which had an additional layer of lithography. PMMA was deposited and exposed only in small windows around the pillars. This prevents nanocrystals from attaching anywhere except in the exposed area. Although I was not able to do this part of the procedure independently, I assisted P.A.G. Astier in the process and

observed every step. I microscoped the device looking for flaws and decided which connections are to be bonded.

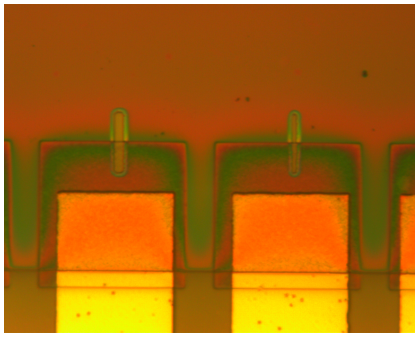

Figure 7: Microscope picture I took displaying pillars with exposed windows. For size reference, thickness of the gold fingers is $80\mu m^2$

Finally, for its properties to be measured, the device needs to be bonded onto a package. Due to an error in the production, we were unable to do this. The device is usually bonded with a wedge bonder which melts and presses a thin gold wire onto the Ti-Au bonding pads on the chip and the package. However, on our device, this process resulted in parts of the bonding pads being broken and lifted off the device. There are several possible reasons why this might have happened. As old does not adhere well to gallium arsenide a layer of Ti is deposited between Au and GaAs layers. This makes gold deposition easier and the connection stronger. If not enough of Ti was deposited or it oxidised before the deposition, it could make the gold not attach well. Also, in case the layer of deposited gold is too thin, it might make the pads too sensitive and bonding impossible.

After attempting several bonding techniques, it became clear that fixing the chip will require more extensive repairs. To make measurements on the device possible, redeposition of gold is required. It will be done using a laser writer to expose the bond pads, etching the existing layer with gold etch and depositing a new Ti-Au layer. However, this will take time and it was decided that I should switch to a different device which still had a similar idea of contacting nanocrystals by sandwiching them between two conducting electrodes.

3.2 Graphene device

The idea behind the device I measured is to use the unique properties of graphene to create an electrical contact with nanocrystals. Most of the fabrication outlined below was done by J.M. Fruhman and H.P.A.G. Astier.

The device is based on PbS nanocrystals sandwiched between Ti/Au and graphene electrodes Fig. (8). Each chip consists of 42 gold fingers with horizontal thickness ranging between $0.8\mu m$ and $4\mu m$ and vertical thickness of 35nm. These are fabricated using the techniques of optical lithography with quartz-chrome mask designed by J.M. Fruhman, Fig.(9). Optical lithography has precision up to an order of $1\mu m$ and the smallest features of the device are pushing it up to the limit, but have successfully been resolved.

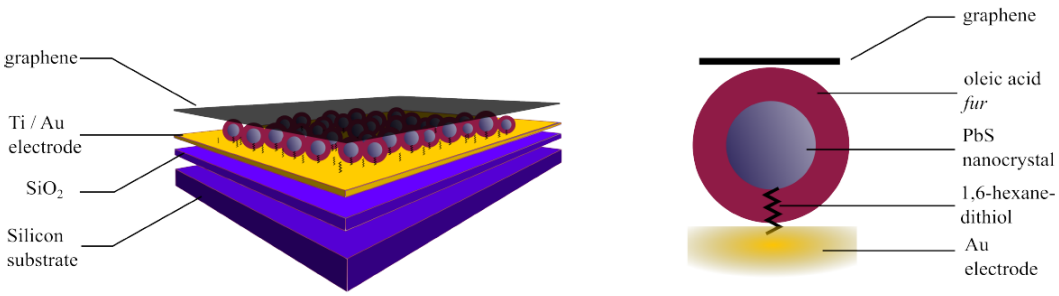

Figure 8: Structure of the device. Left: layered structure of the device. Right: electrically contacting nanocrystal cross section. Picture taken from Ref. [1]

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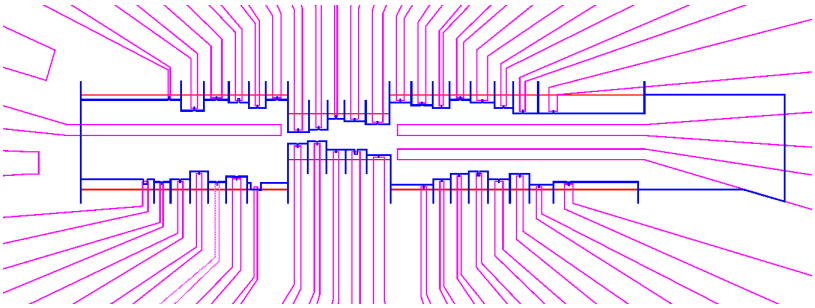


Figure 9: AutoCAD mask design used for optical lithography, realised by J.M. Fruhman. Purple: gold fingers. Red: graphene sheet. Blue: EBM lithography

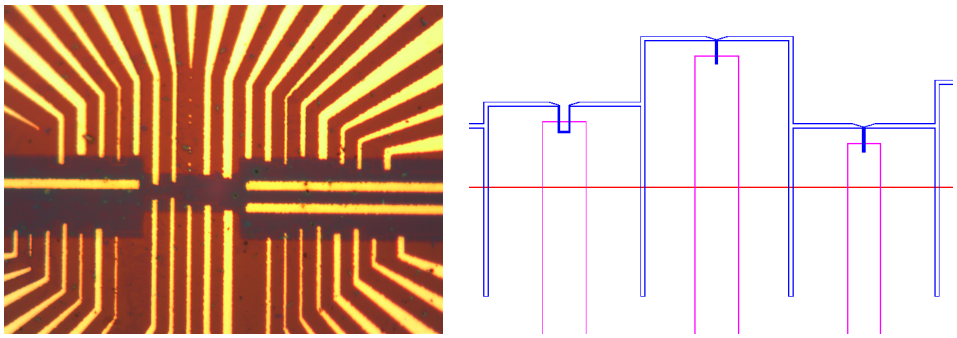
Figure 8 displays the cross section of 39 vertical fingers which are coated with nanocrystals. Horizontal fingers do not contain a layer of nanocrystals and have a direct graphene-Au contact. These are used to ground the device and are referred to as common contacts. On every device, apart from 3 common contacts, 20 junctions are connected. This gives us redundancy in case some of the fingers did not develop correctly or had other flaws.

The electrodes are produced using positive lithography and evaporation on SiO_2/Si substrate. As gold does not adhere well to quartz directly, a 10nm layer of Ti is evaporated prior to 25nm layer of Au.

Once the electrodes have been made, vertical fingers are covered with nanocrystals via a process of self-assembly. A selected region on fingers is exposed with optical lithography and the device is immersed in a solution of 1,6-hexanedithiol (6DT) dispersed in isopropyl alcohol (IPA) for 24 hours. These thiols have an affinity to attach to Au and form dense monolayers [11].

Colloidal PbS nanocrystals of size 4.9 ± 0.3nm are kept in an octane dispersion and are covered in oleic acid fur which prevents them from clustering (see [7] for the growth method). Exposing the chip to the solution of NCs for another 24 hours attaches the crystals to the thiol head forming a strong connection through the fur as shown on the right side of Fig.(8). We get rid of the extra non-attached NCs by spinning the device at the end of the process.

After the NCs are deposited, the whole device is covered in graphene using a wet transfer as described in Sec. (2.1). The graphene layer is patterned with optical lithography and etched with plasma reactive ion etching (RIE) to leave only a small area of fingers covered as shown in Fig. (9).



(a) (b)

Figure 10: Left: picture I took of a finished device prior to measurement. It can be seen that the finger the middle top finger did not develop properly on this device. This is due to errors in optical lithography. Right: AutoCAD design of fingers on graphene developed using EBM

We assumed that the number of conducting NCs will scale with area. Hence, the devices were further refined by electron-beam lithography (EBM) designed to reduce the contact area on the fingers. The precision of EBM is used to carve out fingers in graphene of varying width going down to 10nm (Fig.(10)).

Furthermore, two types of NCs solutions were compared: pure PbS and PbS diluted in ZrO_2 NCs. The latter contained 1 PbS crystal for every 100 ZrO_2. Zirconium oxide particles are 4.6nm in diameter and have a band gap which is roughly 5eV, much bigger than 0.37eV gap in PbS. Hence, it is expected that the crystals with a bigger band gap will effectively act as isolators reducing the number of conducting particles.

4 Methods

4.1 Measurements of the I-V characteristic

As described in Sec.(2), the single-electron phenomena will not be observable unless $k_B T \ll e^2/C$. An estimate of the scales of our system suggests capacitance of order 10^{-17} [16] which requires $T \ll 180K$. Hence, measuring the device in liquid He-4 ($T = 4.2K$) should gives us an environment stable enough to observe nanocrystal charging effects.

I constructed the probe which we used to lower the device in the liquid He-4 dewar and preform the measurements. The probe has a removable chip carrier at the bottom in which the package can be inserted. The chip carrier has 20 connections which correspond to the 20 junctions bonded on the device. These are connected to the head of the probe which is hermetically sealed to prevent leakage of helium from the dewar.

The probe is lowered/raised from liquid He in small steps as rapid changes of temperature might ruin the device. Also, we noticed that even with careful handling, thermally cycling the device by taking it out and inserting it back into liquid He can make the contacts change their behaviour. However, the general form of the I-V curves usually remains the same. Moreover, the probe has to be grounded at all times when the device is inserted and the device should only be handled with tweezers. This is because any static discharge might be enough to damage the sensitive junctions.

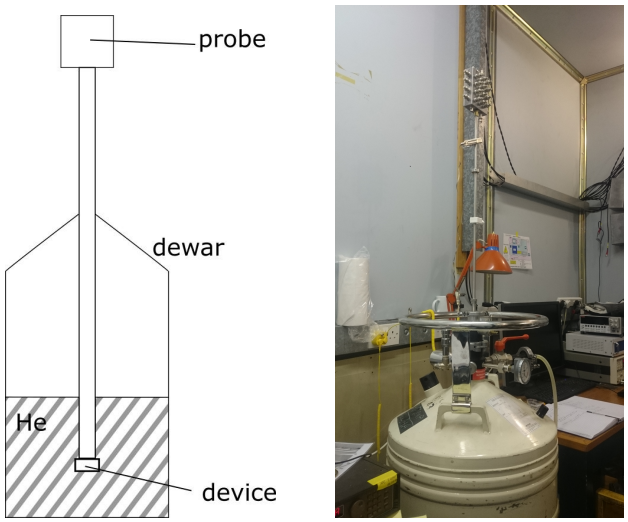


Figure 11: Sketch and a picture of the dewar I used for the measurements

When measuring a particular contact I was making a sweep across the voltage and recording the current through the chip using the program CryoMeas developed by Prof. Ford in the SP group. Because of capacitative forces inside the junction, high voltages can easily damage the device. I start with current compliance of 1nA. If no features are detected, I increase the current compliance iteratively, with a maximum of 500nA for high conducting junctions or junctions which are short-circuited. Moreover, when interesting features are detected, I lower the rate at which the voltage is changed and make multiple sweeps around that region.

Sometimes, when pushed to higher currents, contacts would irreversibly change their behaviour. An example of this can be seen in Fig. (12). Hence, we always have to make sure we have enough measurements on the given current scale before increasing the compliance.

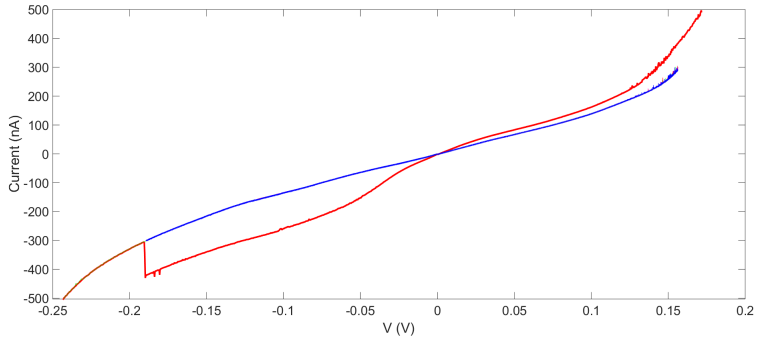


Figure 12: Contact on device EBD40E which displayed change of behaviour. Initially, the behaviour would follow the blue line, but when higher currents were tried, the behaviour abruptly changed to the red line

4.2 Errors

In the I-V characteristic of our device, we can notice very fine features, down to 10pA in size. Due to these small current scales, our measurements are prone to errors introduced by several effects neglected at higher currents. Firstly, as the wires we are using have non-zero capacitance, increasing/decreasing voltage introduces a current offset. This can be seen from:

$$Q = CV \Rightarrow \frac{dQ}{dt} = I = C\frac{dV}{dt} \tag{4}$$

However, this only introduces a constant offset of order 1pA which can be accounted for by taking the average between up and down sweeps across a given voltage range. The effect is most clearly visible in open junctions such as on Fig. (13).

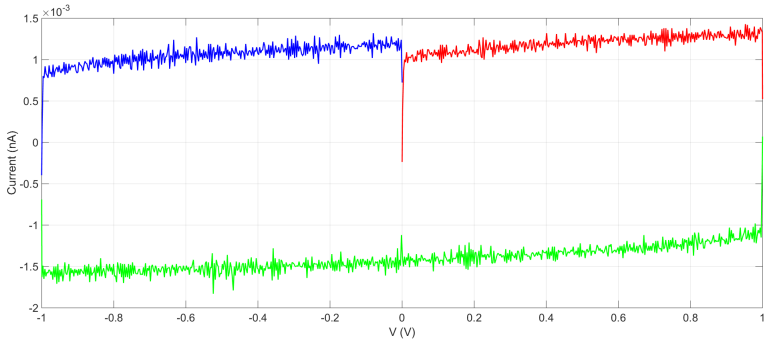


Figure 13: Open contact I measured on the device EBD50A. Data plotted in red and blue was from ramping the voltage up, while the green one was from ramping down. Noise and offset of about 1.2pA due to capacitance of wires are visible.

Moreover, the device is sensitive to disturbances. Small vibrations of the dewar due to touching it or walking in its proximity introduce a visible level of

noise. Care has to be taken to minimise the noise and the motion around the dewar giving us the measurements correct to within about 0.3pA.

5 Results

We can classify the different types of I-V characteristics we observe into several classes. Firstly, a high proportion of junctions has the form of what we refer to as thiol curves, shown in Fig. (14). These types of contacts are characterised by high conductivity, usually reaching current of 100nA at voltages of about 0.05V. However, their average resistance is of order of magnitude larger than in shorted junctions and their characteristic displays polynomial behaviour which asymptotes to a linear curve at high currents. The behaviour is attributed to conductance through linker molecules since it is also displayed by the control devices in which nanocrystals are not deposited and we only have Au-Thiol-Graphene structures.

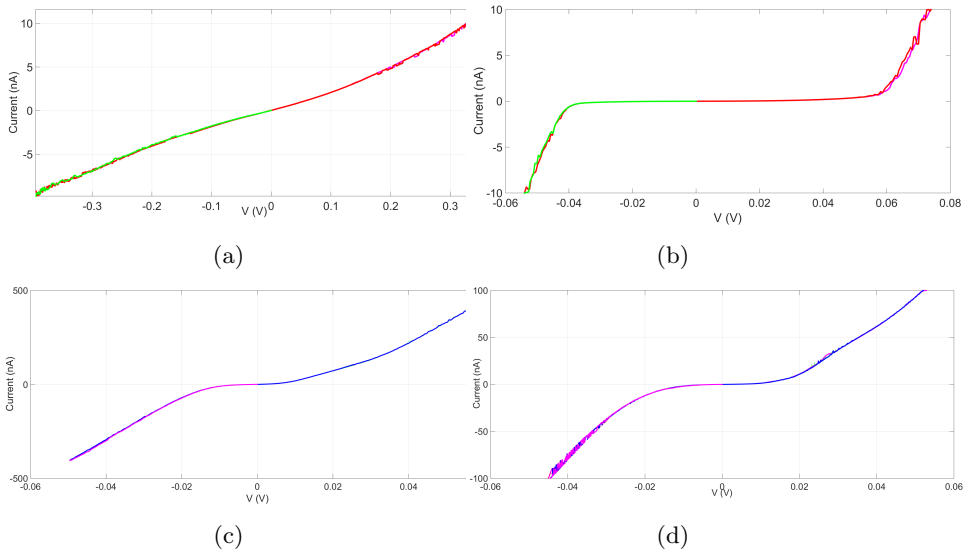
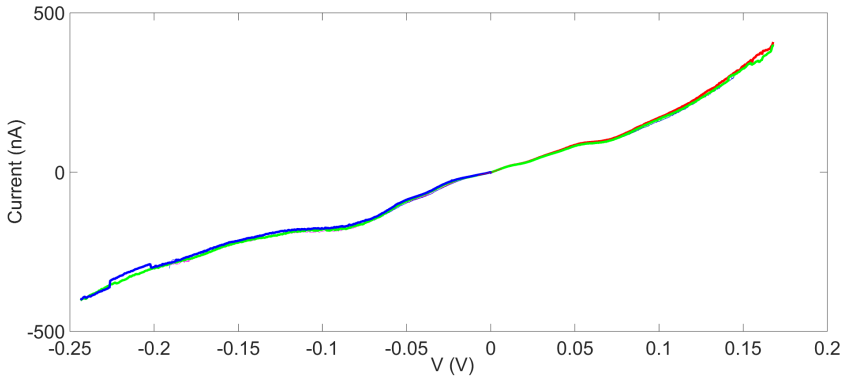


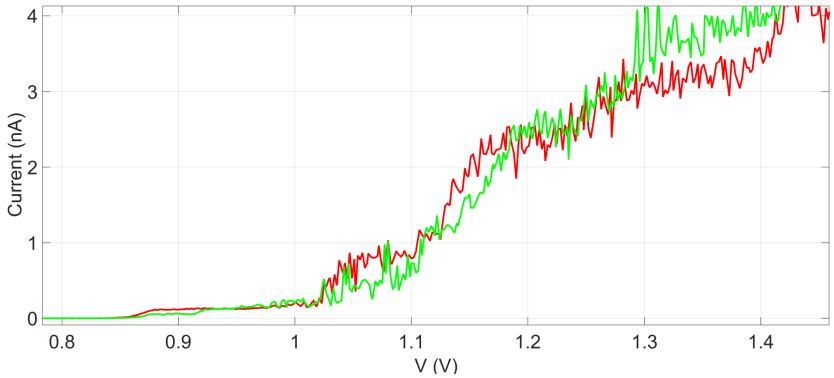
Figure 14: Examples of thiol curves: (a),(b) curves from control devices containing no nanocrystals, (c)-(d) curves I measured

Secondly, we measured contacts exhibiting staircase-like characteristics. As explained by theory in Sec. (2) and supported by the measurements of control devices, this implies conductance through nanocrystals. Examples of these curves can be seen in Fig.(15).

Comparing results gained with two different NC solutions, it was noticed that the pure PbS NCs generally give better results than the diluted samples. We did not manage to measure a staircase as well defined as the one on the Fig. (15c) with diluted samples. On the other hand, every chip with a pure sample had one or more contacts with clearly defined steps. Moreover, junctions with diluted NCs proved more sensitive, often changing behaviour when pushed to higher currents.



(a)



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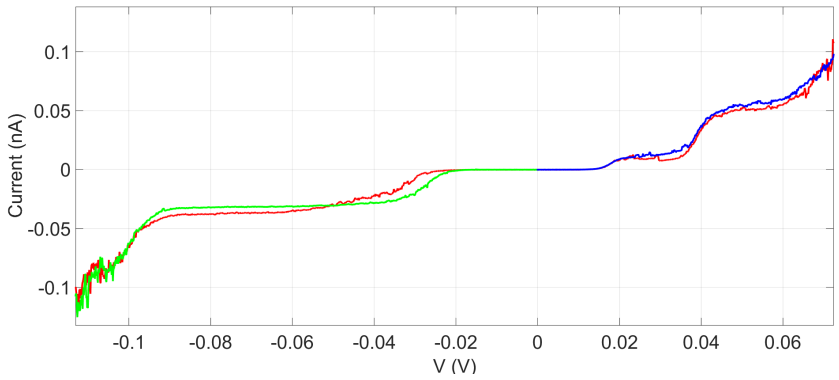

(c)

Figure 15: Examples of curves which suggest conductance through nanocrystals. (a) Thiol curve with changes of gradient, (b) noisy steps (c) best example of staircase I measured. Small differences in positions of steps are expected and result from trapped charges

An interesting feature we observed is switching of channels. It is charac-

terised by fast oscillations of the system between two stable configurations (16). This type of curve is observed in both the nanocrystal and control devices. It usually arises at higher currents and is suggestive of movement of elements in the device such as 'flapping' of graphene due to capacitive forces.

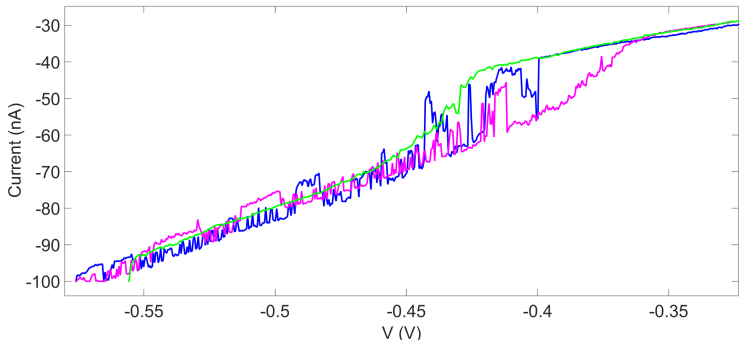

Figure 16: An example of switching of channels

In addition, some contacts displayed a drop in the current when the voltage was increased, referred to as negative differential resistance (NDR). The behaviour is often not reproducible, usually arising due to switching of channels or when the junction is going through a change of behaviour as in Fig.(12). However, in rare cases NDRs are stable. This is not well understood, but most likely implies that the nanocrystals are allowed to move between two or more stable configurations. I measured a very stable example of an NDR which can be seen on Fig.(17).

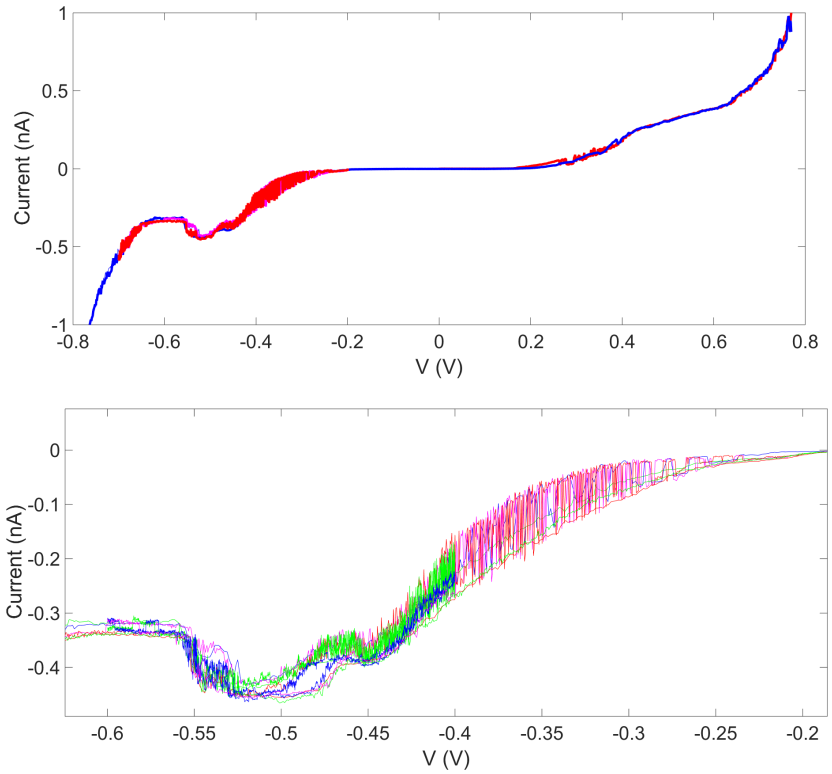

Figure 17: An example of a reproducible NDR I measured. Full curve on the top and zoomed in NDR over many runs on the bottom. It can be seen that the curve has additional step like features and switching of channels around the NDR implying possible nanocrystal charging and a transition to a different stable state.

After measuring four devices and taking into account other previous measurements done by the group, I classified curves in all measured contacts. I compared the area of a junction as defined by the device's design to its average resistance over the measured scale. The latter I took as a ratio of voltage to current for the point with the highest measured current (Fig. (18)). Naturally, due to non-linear behaviour of most contacts, this does not give a precise measure of resistance. However, since the current scales we measure are very different, it can tell us what scale we can expect from a particular type of junction.

Dependence of the current scale and the type of curve on the area of a junction was expected. However, as the gold fingers of the device are made using optical lithography, there can be a deviation in their length big enough to significantly change the nominal area of the overlap with graphene. To find the correction to the area of contacts, electron microscopy pictures of the devices have to be taken. This is yet to be completed and is the next step SP group is going to do to analyse the devices.

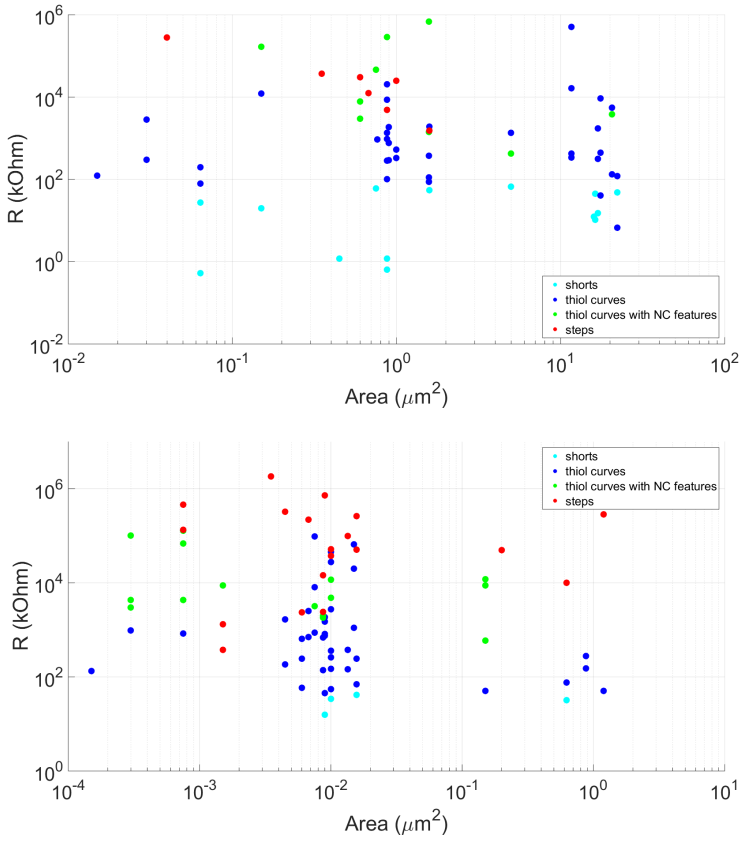

Figure 18: Log-Log plots of average resistance against the nominal area of junctions for different types of curves in devices with diluted NCs samples (top) and pure PbS NCs samples (bottom).

6 Discussion

The types of I-V characteristics that we get agree with what the theory of Coulomb staircase and the measurements of control devices predict. In our chips, we do not have a control over how many nanocrystals are conducting. An estimate based on the density of nanocrystals is that in the smallest junctions the number of nanocrystals goes down to the order of tens of crystals. However, it may be the case that due to a variation in the size of the NCs, only the bigger ones create a contact with graphene.

From Fig. (18) we can clearly see different current scales associated with the type of curve. Short circuits have a resistance lower than 100kΩ while thiol curves have an average resistance between 10^2 and 10^4 kΩ. Contacts with features associated with conductance through nanocrystals usually have a resistance higher than 1MΩ. It is apparent that the pure PbS samples produce fewer shorts and more junctions which are exhibiting nanocrystal curves.

No clear dependence of the conductance or the type of curve on the area can be seen from Fig. (18). In devices with diluted NC solution we only observe

steps in junctions with area lower than $5\mu m^2$, but since the number of contacts with this type of behaviour is small, no definite conclusions can yet be made. The corrections to the area from electron microscopy of chips might give us more insight.

7 Conclusion

From our measurements we can conclude that these types of devices can be used to electrically contact nanocrystals and observe single-electron charging phenomena. However, more work needs to be put into perfecting the design. Specifically, more data and more precise measurements of the area of junctions can tell us which type of junctions are preferred.

Also, it can be concluded that diluting PbS NCs in ZrO_2 leads to a smaller proportion of contacts which exhibits nanocrystal curves. Moreover, it makes the measurements more prone to switching of channels and changes of behaviour, making us believe that the movement of NCs in those device is easier. The reason behind this is not yet completely clear, but we believe that it might be due to a difference in sizes of the crystals in the solution.

The next step in investigating the properties of the Au-PbS-graphene structures is to introduce a gate and observe its effects on the I-V characteristics. The theory predicts that we should be able to control the size of the Coulomb blockade by applying the gate voltage. For this purpose, the mask used to make the device also contains a design for the aluminium oxide gate as shown in Fig. (19).

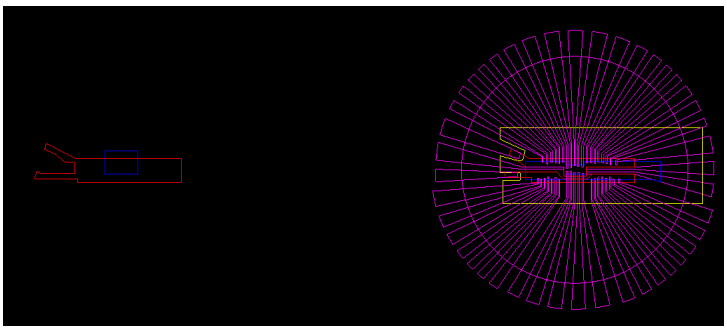

Figure 19: Details of gate design (red) with an insultaor (yellow)

However, initial measurements showed that by depositing Al_2O_3 to the device caused short circuiting of most junctions. It is believed that the reason for this is poor adherence of Au electrode to the insulating layer. Design improvements which would circumvent this are being planned.

The SP group is also working on repairing the device I was initially meant to measure (3.1). It would be interesting to see how two devices compare and which method of contacting self-assembled nanocrystals yields better results. Further research on these types of chips could lead us to the new methods to use self-assembly to effectively contact a small number of nanocrystals and use their unique electrical properties in future technologies.

8 Appendix

8.1 Measuring liquid Helium level

To make sure that the device is indeed in liquid He, I measured tank levels using the effect of thermoacoustic oscillations. Inserting a thin tube with a rubber membrane stretched on top into a dewar results in membrane oscillations. As the gas at the bottom of the tube cools, its density increases and the pressure at the top of the tube falls. Gas from the bottom of the tube then expands into this low pressure region. Under the right conditions of temperature gradient, gas properties and the tube diameter, sustained oscillations can be produced. It has been shown that when the cold end of the tube crosses from vapour to liquid phase, the frequency of the oscillation decreases about 30 percent, and the intensity of the oscillation decreases about 60 percent. With care, helium levels can be measured to within ±1mm using this method [5].

8.2 Additional examples of measured curves

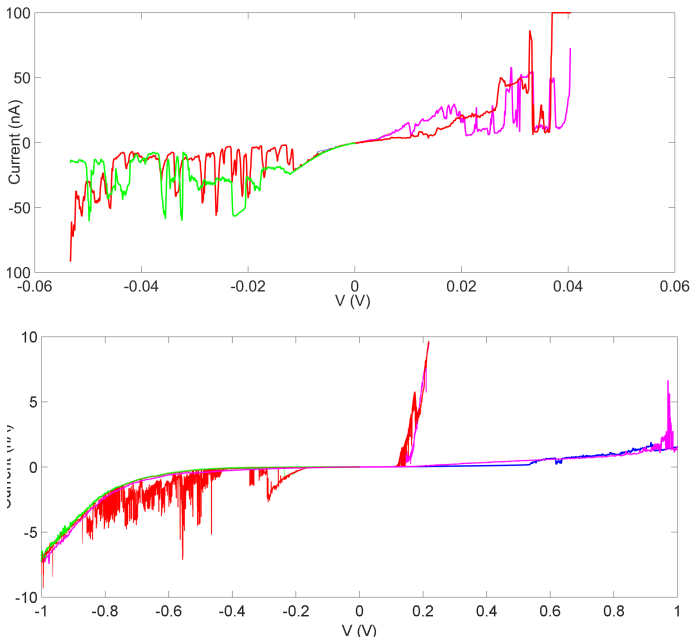

Figure 20: Examples of unstable junctions

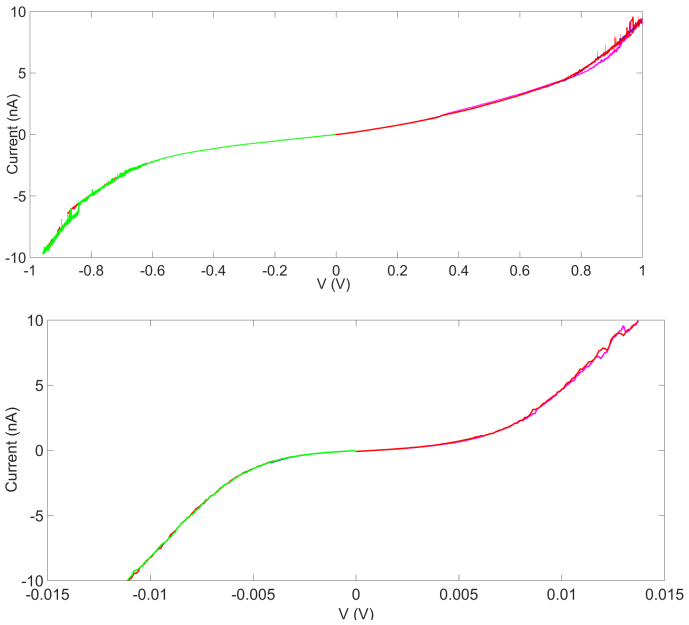

Figure 21: Examples of thiol curves

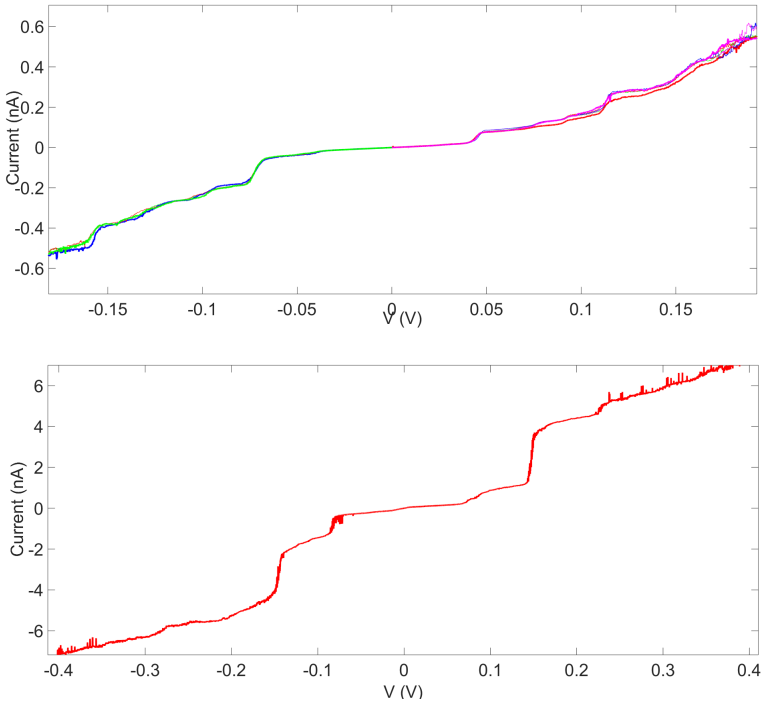

Figure 22: Examples of steps

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